ELSEVIER

Diamond and Related Materials 10 (2001) 744–749

DIAMOND AND RELATED MATERIALS

www.elsevier.com/locate/diamond

Heat-spreading diamond films for GaN-based high-power transistor devices

M. Seelmann-Eggebert[a,*], P. Meisen[a], F. Schaudel[a], P. Koidl[a], A. Vescan[b], H. Leier[b]

[a] *Fraunhofer Institut für Angewandte Festkörperphysik, Tullastr. 72, D-79108 Freiburg, Germany*
[b] *DaimlerChrysler Hochfrequenzelektronik, D-89081 Ulm, Germany*

Abstract

We discuss the potential of heat-spreading films with respect to improving the performance of thermally limited high-power high-frequency GaN-FET devices and report on successful diamond deposition on GaN-FETs. Detailed conditions for process compatibility with GaN-FET technology are discussed and shown to be satisfied by the low-temperature deposition process developed. © 2001 Elsevier Science B.V. All rights reserved.

Keywords: Device modeling; Nucleation; Metal semiconductor field-effect transistor (MESFET); Processing

1. Introduction

Owing to the combination of high cut-off frequencies, breakdown voltages, saturation velocities and operating temperatures, GaN-based field effect transistors (FETs) have a great potential for high-frequency power amplifiers, offering an increase in power output of at least an order of magnitude in comparison with GaAs FETs of comparable device design [1,2]. A limitation of the performance of GaN is the rise in operating temperature caused by heat dissipation, which leads to large leakage currents [3] and reduced channel mobilities [2].

One approach to reduce the operating temperature is to spread the heat from the highly localized source over a larger part of the transistor area. Heat spreading can be achieved by deposition of an electrically insulating but highly thermally conducting film. Distinguished by these film properties, diamond is the material of choice. Owing to its excellent heat conductivity κ, which exceeds 20 W cm^{-1} K^{-1} at room temperature, chemical vapor-deposited (CVD) diamond is used for heat-spreading coolers. Although the thermal conductivity of CVD diamond reduces with decreasing thickness [4], we found it to exceed that of gold, even at a thickness as low as 2 μm.

However, as for the deposition temperature, plasma exposure and non-invasive seeding of the diamond deposition process need to be fundamentally redesigned to satisfy the compatibility requirements of GaN devices. In this paper, we demonstrate experimentally that CVD diamond can be deposited on GaN-FETs without any degradation of the transistor characteristics by fabrication of the first heat-spread transistor prototypes.

Before we report on the technical details of diamond deposition on GaN-FETs, we discuss some results of thermal simulations. The thermal efficiency of the dia-

* Corresponding author. Tel.: +49-761-5159-465; fax: +49-761-5159-400.

E-mail address: Seelmann@iaf.fhg.de (M. Seelmann-Eggebert).

0925-9635/01/$ - see front matter © 2001 Elsevier Science B.V. All rights reserved.
PII: S0925-9635(00)00562-8

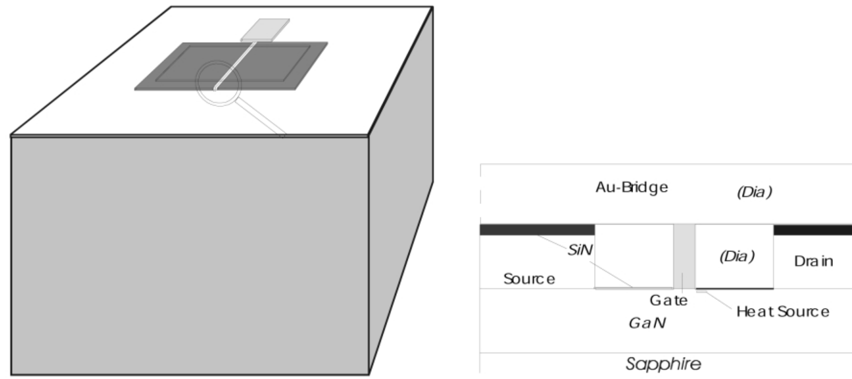

Fig. 1. Sketch of the device geometry: (a) model used for the thermal simulations; and (b) enlarged cross-section of the transistor finger.

mond spreading-layer is analyzed and compared with other approaches to the thermal management of power FETs.

2. Thermal modeling of GaN-FETs

Obtained by dicing a chip from the wafer, a GaN-FET is located on the surface of a cube-like slab. As sketched in Fig. 1, the FET dimensions are much smaller than those of the chip, which therefore have little influence on the thermal device performance. In the FET structure, the heat source is filament-like. Although the filament length is much greater than the thickness of the epilayer, the filament diameter is much smaller, and the heat is practically spread in the plane of the GaN layer. Also, there is already a significant temperature drop in the GaN layer and the device temperature can be less influenced by the choice of the substrate material than expected beforehand. For cost reasons, FET power devices would be preferably fabricated from GaN-structures grown on sapphire rather than SiC substrates, although the latter have a 10-fold higher heat conductivity.

For our model simulations, a chip 500×500 μm^2 in area was chosen. The GaN layer ($\kappa = 1.3$ W cm^{-1} K^{-1}) is assumed to have a thickness of 1 μm and to be grown on a sapphire substrate of 300 μm thickness ($\kappa = 0.46$ W cm^{-1} K^{-1}). In the center of the chip surface was a mesa ($100 \times 125 \times 0.5$ μm^3) with a single-finger FET of gate width 100 μm and gate length 0.25 μm. The gate–source and gate–drain distances were 1 μm each. All contact pads were 90×120 μm^2. Extending from the edge of the gate contact over a distance of 0.15 μm towards the drain, the heat source was assumed to be 25 nm below the surface and to have a height of 15 nm. Heat generation was assumed to be uniform over the heat-source volume [5].

The modeling results are discussed in terms of thermal impedance [5,6] rather then temperature. The local thermal impedance is the temperature rise (as measured with reference to the heat sink) normalized to the heat power dissipated per gate-width unit (as an arbitrarily chosen characteristic device length). To estimate the interdigital crosstalk of multifinger devices, it is convenient to analyze the thermal impedance profile (TIP) of a single FET-finger as a plot along the distance from the center of the finger in the plane of maximum temperature [6] (i.e. a line just below the GaN surface in the cross-section of Fig. 1b). Since the TIPs of different fingers are very similar, the temperature profiles over a comb of fingers can be obtained from a single TIP by lateral translation and subsequent superposition. The introduction of the TIP is useful owing to two simple scaling rules for stationary heat flow: for a considered thermal-impedance profile the temperature is proportional (a) to the heat load and (b) to the reciprocal gate width, if the whole geometry is rescaled with no change in shape. The peak temperature in the device is obtained by multiplying the peak impedance with the heat dissipated per gate-width unit.

The curves shown in Fig. 2 are thermal simulation

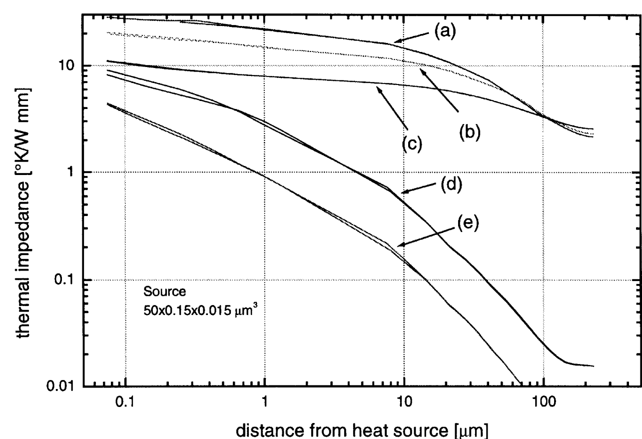

Fig. 2. Thermal impedance profiles of GaN-FETs for different thermal setups: (a) bare finger; (b) 3-μm gold bridge as thermal shunt; (c) 3-μm diamond spreading layer; (d) gold bridge in flip-chip geometry; and (e) spreading layer in flip-chip geometry. In (a)–(c), the heat sink is at the substrate bottom, in (d) and (e) at the top.

results for the single-finger device sketched in Fig. 1a operating under different thermal conditions. Despite the asymmetric position of the heat source with respect to the gate contact, differences in the left and right branch of the curves in Fig. 2 are negligibly small.

The uppermost curve represents the situation of the GaN-FET finger without any thermal precaution. The peak thermal impedance, $R_o = 29.5$ K mm W^{-1}, obtained by the simulation is only approximately half the value predicted by the Smith formula for the considered heat source geometry embedded in a sapphire matrix [5]. Hence, the GaN epilayer, with a comparatively high thermal conductivity itself, results in a significant reduction in the operating temperature. In Fig. 2a, the heat-spreading effect of this layer is seen as a broad appearance of the TIP and a slow decrease at large distances x from the gate ($\Delta T \sim 1/\sqrt{x}$). This behavior implies a comparatively strong thermal coupling between multiple FET fingers if placed at a typical distance of 30 μm: the respective coupling impedance R_c is approximately one third of R_o.

Conventional thermal shunts are formed by thick gold–air bridges ($\kappa = 3$ W cm^{-1} K^{-1}) attached to the gate contact and a large fraction of the chip area. In our model calculation, the gold bridge was 3 μm thick and (as sketched in Fig. 1b) connected to the large drain and source contact pads via a 0.2-μm thick insulating SiN layer ($\kappa = 0.016$ W cm^{-1} K^{-1}). The thermal design reduces the thermal peak impedance to 70% of its initial value, however, the coupling impedance is lowered only by 10% (Fig. 2b). Hence, the situation regarding thermal crosstalk is not improved.

A drastic temperature reduction is found if a closed spreading layer of diamond is deposited (by use of $\kappa = 3$ W cm^{-1} K^{-1}, fine-grained CVD diamond of poor thermal quality is assumed). Protecting the exposed surface areas of the transistor, a 20-nm thick SiN layer was included in the calculation. The thermal impedance peak is reduced to 40% of the original value, but the R_c/R_o ratio increases further. The large improvement in R_o with respect to the thermal-shunt approach is a consequence of the lateral distance of the heat source and gate contact. Covering the heat source completely, the film bridges this gap.

Appreciable thermal crosstalk is common to the three considered situations (Fig. 2a,b,c) and results from the position of the heat sink at the bottom of the substrate, i.e. in the thermal far field. Flip-chip designs bear an appreciable advantage over backside-cooled spreading or shunt designs, if the sink can be placed in the near field and, consequently, crosstalk is substantially reduced. Although technically impossible to realize, it is instructive to place the heat sink directly on top of the bridge or spreading layer. The gold bridge design with topside cooling brings the R_c/R_o ratio down to 0.02, although the peak temperature reduction is approximately the same as for the diamond spreading-layer with backside cooling. If a respective flip-chip set-up could be realized with the use of a closed spreading-layer, the temperature rise during operation could be reduced by a factor of 5.2 with a crosstalk ratio R_c/R_o of 0.01.

In practice, the apparent advantages of the flip-chip approach are less pronounced. Since relatively thick thermal bumps are required to mediate the bonding of the heat sink to the chip surface, the device temperature is lowered by heat spreading in the thermal bumps rather than by near-field heat flow to the sink. Nevertheless, to achieve high cooling efficiencies, both thermal management approaches require coupling of the film to a large area over the heat source — a condition much easier to satisfy with a dielectric than with a metal.

3. Process requirements

In view of its superior thermal and dielectric properties, CVD diamond appears to be the material of choice for heat-spreading applications. However, hostile conditions for deposition impede this application of CVD diamond on delicate semiconductor devices. High quality diamond is obtained in a methane/hydrogen plasma at elevated deposition temperatures (800°C). Deposition at lower temperatures is possible, but brings about losses of quality and low growth rates [7]. For GaN devices, which are themselves grown at temperatures near 1000°C, a temperature of 500°C appeared to be an appropriate upper limit for diamond deposition, mainly implied by stability considerations of the FET contacts. On silicon substrates, we realized and routinely grow diamond films at this temperature, with thermal conductivities exceeding that of gold (3 W cm^{-1} K^{-1}), a thickness > 3 μm and growth rates of 0.2 μm h^{-1}. However, on epitaxial GaN films, diamond deposition is impossible, due to rapid GaN etching (> 1 μm h^{-1}) in the plasma, with the eventual formation of gallium droplets. A further problem may occur for p-doped material, by rapid diffusion of atomic hydrogen from the plasma into the GaN matrix.

4. The protective layer

In view of the obvious instability of GaN in the CVD plasma, the question arises as to how diamond films can be deposited on GaN-based FET devices. However, this apparent obstacle can be overcome by the use of a suitable protective layer satisfying the following requirements. The protective layer should be plasma-resistant and impervious to hydrogen. With regard to the high-temperature cycle employed, it should show

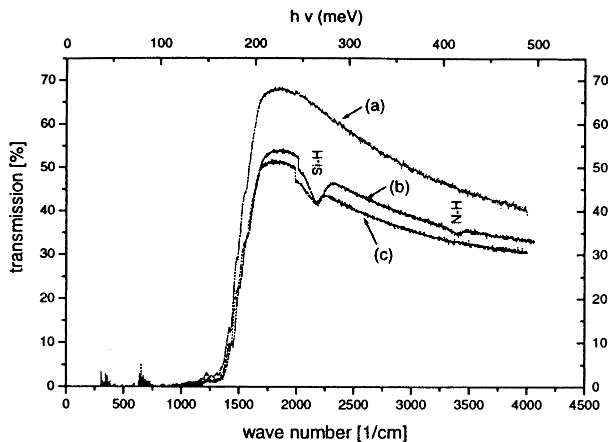

Fig. 3. IR transmission spectra of: (a) plane 300-μm sapphire substrate; (b) 500 nm SiN on sapphire after 30-min CVD plasma exposure; and (c) same layer after 2-h vacuum annealing at 550°C.

good adhesion properties to GaN and diamond. Seeding properties of the protective layer are important for stability and seed formation. High heat conductivity is desirable, although not necessary, if plasma protection is warranted, even at a very small thickness of the interlayer.

AlN, SiO_2 and SiN layers were investigated and found to satisfy these requirements, but SiN was finally chosen, mainly in view of process compatibility for the entire device fabrication. Crystalline Si_3N_4 has a heat conductivity of 0.3 W cm^{-1} K^{-1}; however, for thin microcrystalline films, much lower values are reported [8]. Measurements on CVD-SiN layers routinely used in the standard fabrication process yielded a conductivity of 0.016 W cm^{-1} K^{-1} [9]. Even upon long-term exposure (10 h), films of this CVD-SiN material were not etched by the deposition plasma.

However, SiN films of 0.1–0.2 μm thickness showed a trend of wrinkle formation after prolonged exposure, indicating local delamination [10]. IR transmission studies implied some migration of atomic hydrogen through the SiN films. After plasma exposure, absorption features corresponding to Si–H and N–H stretching vibrations are observed, indicating that hydrogen is trapped in the SiN layer (Fig. 3). The hydrogen features are appreciably diminished upon annealing in vacuum. Hydrogen diffusion is likely to be much less efficient in the active parts of the device, since these become quickly passivated by the growing diamond overlayer.

5. Seeding

Appropriate seeding is required to achieve a high nucleation density and to rapidly form a closed diamond film. Common seeding procedures, such as mechanically polishing with diamond powder, are not suited for structured micro-devices. We therefore attempted to seed by means of an ultrasonic treatment in a dispersion of diamond powder in water or methanol. This approach yielded generally high nucleation densities (in the order of 10^{10} cm^{-2}) with good uniformity, even over edges of the device structure, and facilitated quick overgrowth of the GaN device. However, the protective SiN coating was found to be damaged by this treatment, even when the treatment was short and diamond powder with a sub-μm particle size was used. After a few minutes of plasma exposure, the surface appearance of ultrasonically seeded samples became spotty and the SiN film was observed to peel off locally at these spots.

Ultrasonic seeding was also found to deteriorate the transistor performance. At the typical pinch-off voltage of 6 V, large leakage currents of approximately 10% of the saturation current were found after the ultrasonic treatment. The observed change in the electrical characteristics indicated damage of the gate electrode caused by the impact of fast diamond particles.

Owing to the failure of the conventional approaches, an alternative non-invasive seeding method was developed, based on the sedimentation of fine diamond particles from an agitated emulsion. An advantage of this technique is its independence from the surface properties of the substrate. With this seeding technique, very homogeneous and uniform diamond films have been grown on 2-inch wafers of silicon and glass.

To achieve a selective area growth for diamond films, the sample surface was structured by selective seeding. To avoid diamond growth on specific areas, such as the contact pads, these were covered by photoresist. After the seeding procedure, the photoresist was dissolved in hot acetone or dimethylformamide. The seed layer was completely removed with the photoresist. Hence, diamond grew only on the exposed areas of the samples, whereas unseeded regions remained practically free of deposits.

6. The deposition process

Diamond deposition was performed in a plasma-CVD ellipsoid reactor [11] operating at 2.45 GHz with a microwave power up to 6 kW and a power density of 100 W cm^{-3}. The sample was located at the bottom of the reactor on a water-cooled stage. The deposition temperature was adjusted by variation of the process pressure or heat-resistance of the stage. For low-temperature deposition, a pressure in the range 70–110 mbar was chosen. At higher pressures, the heat flux density exceeded a critical value, causing thermal cracking [12] of the thin 2-inch sapphire substrates due to temperature inhomogeneities.

Low-Temperature nucleation of the film proved to be a critical step. To form a closed film within a period of no longer than 10 min, a temperature of at least 500°C (as measured by a pyrometer operating at a wavelength of 1000 nm) and a largely increased concentration of methane (4%) was required. After successful nucleation (as monitored by interferometry), the methane content of the process gas was set to 1% and, optionally, the temperature was reduced. The following parameters are a typical example of the process conditions: at a pressure of 80 mbar, the heat flux density at the sample surface was 30 W cm^{-2}. If the deposition temperature of 500°C is adjusted by a suitable choice of the thermal resistance of the stage, a growth rate of 0.25 μm h^{-1} is obtained.

Adhesion of the diamond films was problematic if a large-area deposition was attempted. If the thickness exceeded approximately 1 μm, spontaneous flaw formation was observed and the diamond film delaminated as a result of compressive thermal stress built up during cooldown. Somewhat surprisingly, the diamond films turned out to adhere very well on selectively seeded FET samples. On the structured chips, adhesion was aided by separation grooves which were left unseeded and defined individual spreading layers for each FET.

With the process developed, diamond spreading layers were routinely deposited on GaN-FETs. As demonstrated by the REM image of Fig. 4, the diamond layer is distinguished by very good selectivity and exhibits remarkably abrupt edges at the contacts.

The devices investigated in this study were fabricated using a standard GaN-transistor process with gates defined by optical lithography. More details on the fabrication process are found elsewhere [13].

For checks on the compatibility of the CVD-diamond deposition with the overall FET fabrication process, a piece of a wafer was electrically DC characterized before diamond deposition and the protective layer was then put down. Next, areas to be excluded from deposition (such as the contact pads) were covered with photoresist. After selective seeding, the diamond film was grown. The protective layer was then removed from the contacts by dry etching in a CF_4/O_2 plasma and the FET characteristics were recorded for a second time. Fig. 5 shows a comparison of the output and transfer characteristics before and after diamond deposition at a deposition temperature close to 400°C. Fig. 5 demonstrates a well-working transistor, which was subject to only minor alterations in the process of diamond deposition. However, above 440°C, serious degradation of the Ni/Au gate contact occurred, leading to failure of the transistors. EDX measurements revealed that this deterioration had to be attributed to alloying, which caused the gate contact to lose its Schottky character. With an improved GaN-FET processing scheme, stable device operation was accomplished, even at temperatures above 510°C. In the absence of gate-metal alloying phenomena, no signs of transistor degradation after diamond deposition were found. However, for stable gate contacts, an increase in Schottky barrier height was observed after the plasma treatment, an effect typical for heat-treated GaN transistors, caused by an interfacial reaction between the gate metal and the semiconductor.

In a recent run, transistors with the new stable Schottky contacts were investigated at a deposition

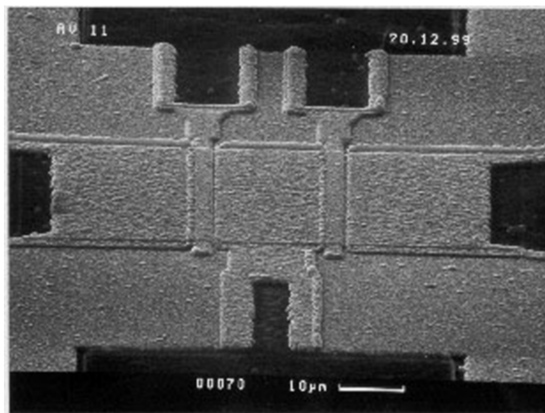

Fig. 4. REM image of a two-finger GaN-FET with a 0.7-μm diamond film (deposition temperature 440°C).

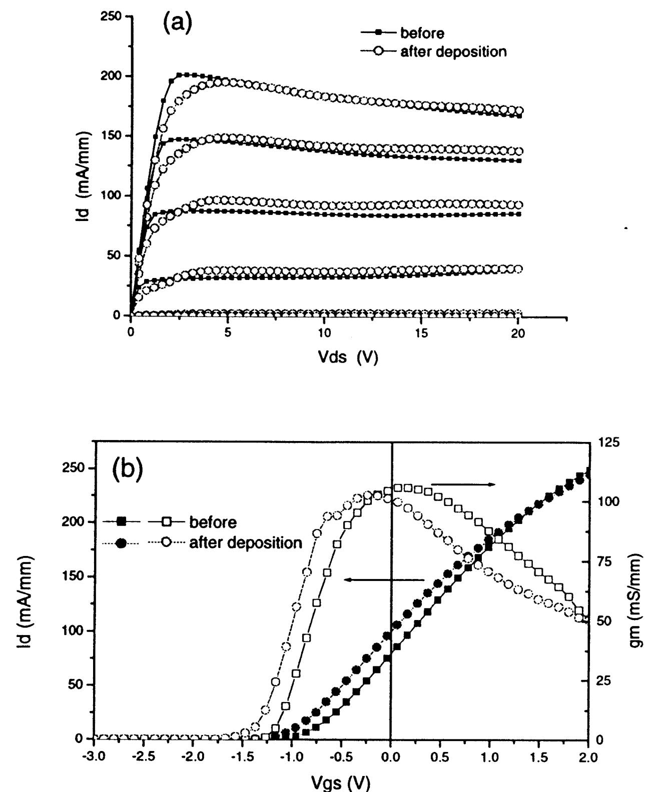

Fig. 5. (a) Output; and (b) transfer characteristics of a two-finger GaN-FET before and after deposition of a 0.7-μm thick diamond film.

temperature of 480°C. Even after deposition of 2-μm diamond, the FETs remained fully operational.

7. Summary and outlook

Heat-spreading diamond films are shown to be an useful approach to reducing the operating temperature of GaN-FETs and, hence, to have the potential for boosting power output of high-frequency GaN devices. Direct CVD deposition of diamond on GaN-FETs is demonstrated to be feasible and completely compatible with state-of-the-art GaN device-processing technology. To achieve this compatibility, a novel gentle seeding process and a low-temperature ($<500°C$) deposition process was developed, involving a protective layer. Temperature-resistant gate contacts are required to allow the deposition temperature to exceed 500°C. To our knowledge, this is the first demonstration of successful CVD diamond deposition directly on an operational III–V semiconductor circuit. Detailed experiments proving the cooling efficiency of the spreading diamond still remain to be performed.

Acknowledgements

H. Güttler and M. Hirsch of DaimlerChrysler and E. Wörner, C. Wild and R. Sah of Fraunhofer IAF are gratefully acknowledged for helpful discussions. This work was supported by the BMBF.

References

[1] Y.-F. Wu, B.P. Keller, S. Keller et al., IEICE Trans. Electron. E82-C (11) (1999) 1895.
[2] C.E. Weitzel, Institue of Physics Conference Series, 142, (1996) 765 (chapter 4).
[3] E. Kohn, W. Ebert, A. Vescan, Isr. J. Chem. 38 (1998) 105.
[4] E. Wörner, in: B. Dischler, C. Wild (Eds.), Low-Pressure Synthetic Diamond, Springer-Verlag, Berlin, 1998, p. 137 (chapter 9).
[5] R. Anholt, Electrical and Thermal Characterization of MESFETs, HEMTs and HBTs, Artech, Norwood, 1994, pp. 58–63.
[6] R. Anholt, Solid State Electron. 42 (1998) 849.
[7] Y. Muranaka, H. Yamashita, H. Miyadera, Diamond Films Technol. 5 (1995) 1.
[8] S.R. Mirmira, L.S. Fletcher, J. Thermophys. Heat Transfer 12 (2) (1998) 121.
[9] H. Güttler, personal communication.
[10] G. Gille, B. Rau, Thin Solid Films 120 (1984) 109.
[11] M. Füner, C. Wild, P. Koidl, Surf. Coat. Technol. 116–119 (1999) 853.
[12] K.J. Gray, H. Windischmann, Diamond Relat. Mater. 8 (1999) 903.
[13] A. Vescan, R. Dietrich, A. Wieszt et al., Institute of Physics Conference Series, 166, (1999) 503 (chapter 7).